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# (54) Dual beam spectrophotometer

(57) An absorbance-measuring system for a dual-beam spectrophotometer (1) comprises a sample cell 19, a reference cell 16, a beam chopper disc (Fig. 2) and a logarithm circuit (33) for providing a signal proportional to logarithm of the composite signal containing reference pulses $V_R$ and sample pulses $V_S$ from a photomultiplier (17). A first sampling circuit (39) controlled by gating signals from a detector array 133 in association with an encoder disc 25 and a light source 132 and a second sampling circuit (40) produce signals proportional to $\log_{10} V_R$ and to $\log_{10} V_S$. A difference circuit connected, as shown (47) produces signal proportional to the absorbance of the sample. Because low level signals prior to an amplifier (35) connected as shown follow a common path, error components due to low frequency noise and drift in the logarithm circuit (33) are common mode and cancel in the difference circuit (47).

The system may further comprise (see Fig. 8) a calibration signal generator (75), log calibration signal sampling circuits (90, 91, 92), a control circuit (93, 94) for controlling the gain of the amplifier (35) and means (98, 99) for producing a signal fed back to the logarithm circuit (33) to compensate offset voltages.

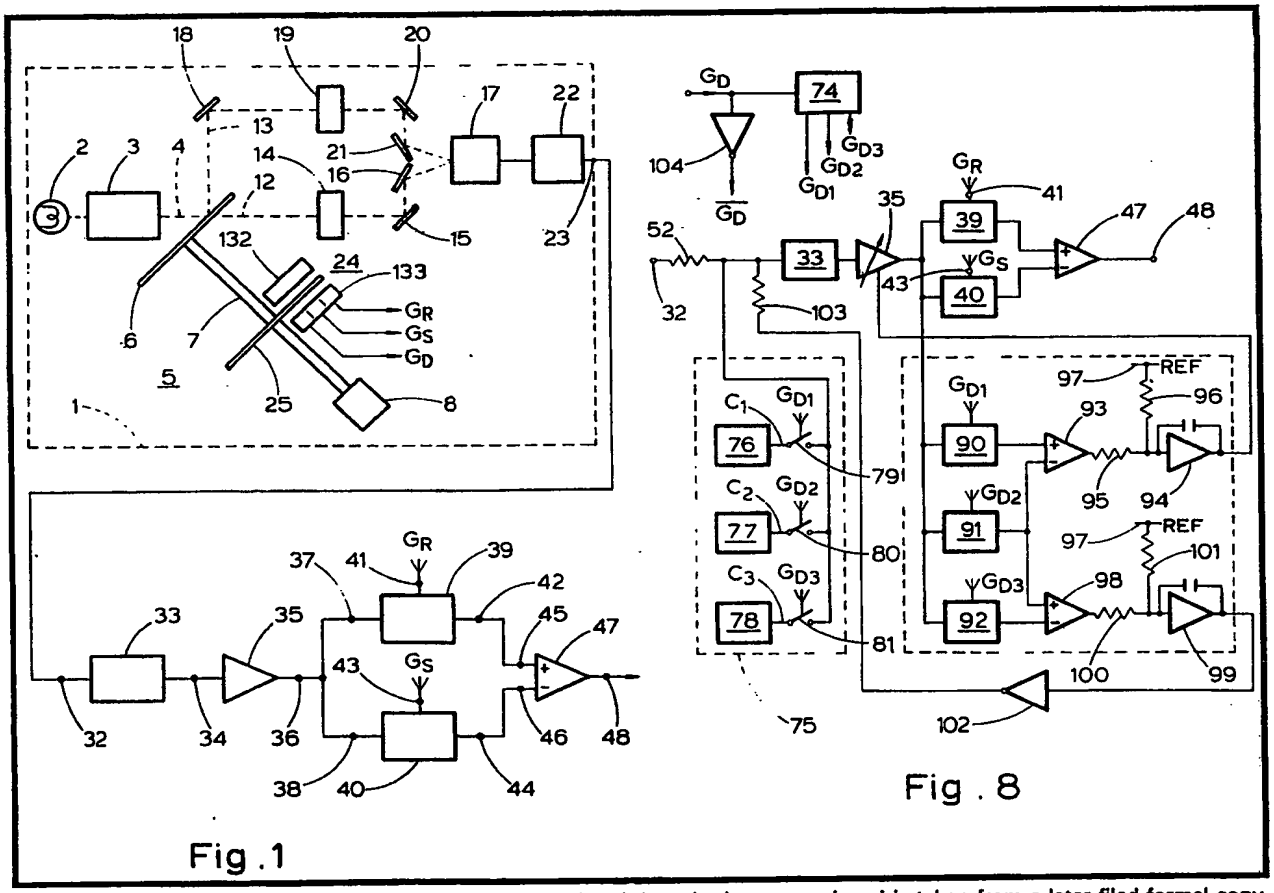


Fig. 1

Fig. 8

SPECIFICATION

**Spectrophotometer**

The invention relates to a dual beam spectrophotometer including a processing circuit for processing a signal produced by a radiation detector of the spectrophotometer to obtain a further signal representative of the absorbance of a substance contained in a sample cell of the spectrophotometer.

In a dual beam spectrophotometer, a beam of substantially monochromatic radiation is split, e.g. by a mechanical "chopper" device into a series of radiation pulses separated by dark intervals.

The radiation pulses are directed alternately along first and second optical paths, the first path passing through a reference cell and the second path passing through a sample cell. After passing through their respective cells, the two paths converge upon a common radiation detector, typically a photomultiplier.

The radiation detector therefore receives a first train of radiation pulses which have passed through the reference cell and a second train of radiation pulses which have passed through the sample cell, the pulses of the two trains being interlaced, and being separated by the dark interval.

The radiation detector produces at its output a composite signal comprising two interlaced trains of electrical pulses corresponding to the two trains of radiation pulses. The amplitude $V_R$ of the pulses of the train (hereinafter the reference pulses train) is dependent on the intensity $I_R$ of the radiation pulses reaching the detector through the reference cell, and the amplitude $V_S$ of the pulses of the other train (hereinafter the sample pulse train) is dependent on the intensity $I_S$ of the radiation pulses reaching the detector through the sample cell. Between pulses of the composite signal, the detector output has an amplitude $V_D$ (the dark level) corresponding to the intervals between pulses when the beam of radiation is interrupted by the chopper and no radiation reaches the detector through either the reference or the sample cell.

To measure the absorbance of a substance, a sample is dissolved in a suitable solvent and placed in the sample cell. Pure solvent is placed in the reference cell. The arrangement is such that any difference in the intensities $I_R$ and $I_S$ is due to the presence of the sample material.

In these circumstances, the absorbance A of the sample material is given by the relationship $A = \log_{10} I_R/I_S$. Therefore,

$A = \log_{10} I_R - \log_{10} I_S = \log_{10} (V_R - V_D) - \log_{10} (V_S - V_D)$ and if $V_D = 0$, $A = \log_{10} V_R - \log_{10} V_S$.

In the processing circuit commonly employed to derive from the composite signal at the output of the radiation detector a signal representative of the absorbance of a sample material the composite signal is first applied to a d.c. restoration circuit arranged to clamp the dark level at ground potential (i.e. to make $V_D = 0$), and then the d.c.–restored signal is applied to corresponding inputs of first and second sample and hold circuits. The circuits receive enabling signals derived from the chopper such that the first sample and hold circuit samples only pulses of the reference train and the second sample and hold circuit samples only pulses of the sample train. The output of the first sample and hold circuit is a d.c. signal whose magnitude $V_R$ corresponds to the amplitude of the reference pulses. This signal is applied to a reference logarithm circuit which produces an output signal $\log_{10} V_R$. Similarly, the output of the second sample and hold circuit, which is a d.c. signal whose magnitude $V_S$ corresponds to the amplitude of the sample pulses, is applied to a sample logarithm circuit which produces an output signal $\log_{10} V_S$. The output signals $\log_{10} V_R$ and $\log_{10} V_S$ are applied to respective inputs of a differencing circuit which produces a signal representative of $\log_{10} V_R - \log_{10} V_S$, i.e. a signal representative of the absorbance A of the sample.

Dual beam spectrophotometers are commonly required to be capable of measuring absorbance over a range extending from $A = 0$ to not less than $A = 3$. Consequently, the logarithm circuits of the above-described processing circuit are required to accept input signals whose amplitudes may vary over a range of at least three decades.

There are several factors which tend to limit the accuracy with which absorbance can be measured by such a processing circuit. One such factor is that the operational signal levels in the logarithm circuits and the differencing circuit tend to be low, and that, typically, the output signal of a logarithm circuit based on the voltage/current relationship of a semiconductor diode junction will change by less than 100mV for each decade change in its input signal. Consequently, the effects of low frequency noise, e.g. flicker noise, and of drift in amplifiers and other components of the two logarithm circuits and the differencing circuit may be significant when compared with the small wanted signals and therefore impose a limit on the accuracy of measurement. Two other such factors are that the gain of a logarithm circuit based on the voltage/current relationship of a semiconductor diode junction is dependent on the temperature of the junction, and that any offset voltages associated with the junction will distort the log law characteristic at small input signal levels. It is therefore difficult to arrange that the characteristics of the reference logarithm circuit and the sample logarithm circuit are matched over

the entire range of operating temperatures and input signal amplitudes. Any mismatch imposes a further limit on the accuracy of measurement.

An object of the present invention is to provide a dual beam spectrophotometer including a processing circuit for measuring absorbance with improved accuracy compared with the above-described commonly employed circuit having regard to at least the first above-discussed limiting factor.

According to the invention there is provided a dual beam spectrophotometer comprising a detector for radiation received from a radiation source via a first path including a reference cell and via a second path including a sample cell, the radiation received via the first and second paths being in the form of interlaced pulses separated by periods in which no radiation reaches the detector via either path, the detector producing a first signal comprising a first train of pulses of amplitude corresponding to the intensity of radiation received via the first path and a second train of pulses of amplitude corresponding to the intensity of radiation received via the second path, the pulses of the first and second trains being interlaced and being separated by the said periods, means for clamping the first signal at a reference level during the said periods to produce a second signal, and a processing circuit for processing the second signal to obtain a further signal representative of the absorbance of a substance contained in the sample cell, characterised in that the processing circuit includes means for producing a third signal representative of the logarithm of the amplitude of the second signal, means for amplifying the third signal to produce a fourth signal, means for sampling the fourth signal to produce a fifth signal representative of the logarithm of the amplitude of the pulses of the first train, and a sixth signal representative of the logarithm of the amplitude of the pulses of the second train, and means for producing said further signal as a seventh signal representative of a difference between the fifth and sixth signals.

In the above arrangement, any error components due to low frequency noise and/or drift in the low signal level stages, i.e. prior to reaching the means for amplifying the third signal, will be common-mode signals and hence will be rejected by the means for producing the seventh signal.

The spectrometer may comprise means for generating upper and mean calibration signals having respective amplitudes corresponding to an upper limit and a mean limit of a range of pulse amplitudes of the second signal, means for applying the calibration signals to an input terminal of the means for generating the third signal, further means for sampling the fourth signal to produce an eighth signal representative of the logarithm of the amplitude of the upper calibration signal and a ninth signal representative of the logarithm of the amplitude of the mean calibration signal, means for producing a tenth signal representative of a difference between the respective magnitudes of the eighth and ninth signals and means responsive to the tenth signal for controlling the gain of the means for amplifying the third signal so as to maintain the magnitude of the tenth signal substantially constant. The magnitude of the tenth signal in this arrangement is very sensitive to the gain of the logarithm circuit, i.e. the means for sampling the fourth signal, and the means for controlling the gain of the means for amplifying the third signal maintains the overall gain substantially constant despite any changes in the gain of the logarithm circuit with temperature.

The spectrometer may comprise means for generating mean and lower calibration signals having respective amplitudes corresponding to a mean limit and a lower limit of a range of pulse amplitudes of the second signal, means for applying the calibration signals to an input terminal of the means for generating the third signal, further means for sampling the fourth signal to produce an eighth signal representative of the logarithm of the amplitude of the mean calibration signal and a ninth signal representative of the logarithm of the amplitude of the lower calibration signal, means for producing a tenth signal representative of a difference between the respective magnitudes of the eighth and ninth signals and means responsive to the tenth signal for generating an eleventh signal effective when applied to the input of the means for generating the third signal to maintain the magnitude of the tenth signal substantially equal to a predetermined value. The magnitude of the tenth signal in this arrangement is very sensitve to residual offset voltages in the logarithm circuit, i.e. the means for sampling the fourth signal, and the means for maintaining the tenth signal at a constant value thus compensates for these residual offset voltages.

In order that the invention and the manner in which it is to be performed may more readily be understood, embodiments thereof will be described, by way of example, with reference to the accompanying drawings, of which:—

*Figure 1* is a block schematic diagram of a dual beam spectrophotometer incorporating a signal processing circuit according to the invention,

*Figure 2* is a diagram illustrative of a beam chopper disc for use in the spectrophotometer of Fig. 1,

*Figure 3* is a diagram illustrative of an optical encoder disc for use in the spectrophotometer of Fig. 1,

*Figure 4* illustrates waveforms at various poits in the processing circuits shown in Figs. 1 and 8,

*Figure 5* is a detailed schematic diagram of a logarithm circuit for use in the processing circuits of Figs. 1 and 8,

*Figure 6* is a detailed schematic diagram of a variable gain amplifier for use in the processing circuit of Fig.8,

*Figure 7* is a detailed schematic diagram of a sample-and-hold circuit for use in the processing circuits of Figs. 1 and 8,

*Figure 8* is a block schematic diagram of the signal processing circuit of Fig. 1 with the addition of self-calibration means,

*Figure 9* is a detailed schematic diagram of calibration signal generating means for use in the processing circuit of Fig. 8.

Referring first to Fig. 1, the basic optical elements of a dual beam spectrophotometer are represented schematically within the broken rectangle 1, and comprises a light source 2 from which radiation having a range of wavelengths passes to monochromator 3. A beam 4 of substantially monochromatic radiation emerges from the monochromator 3 and is incident upon a beam splitting device (chopper) indicated generally by the reference numeral 5. The chopper 5 comprises a disc 6 mounted upon a shaft 7 for rotation therewith. The shaft 7 is rotated by a motor 8.

At least an outer annular portion of the disc 6 is divided into *n* sectors where *n* is a multiple of 4, successive sectors being transparent, absorbent, reflecting and absorbent to the radiation. A typical arrangement is illustrated in Fig. 2, in which an outer annular portion of the disc 6 comprises eight sectors. Two diametrically-opposed sectors 9, 9′ are removed to leave corresponding gaps in the outer annular portion of the disc 6. Two further diametrically opposed sectors 10, 10′, disposed orthogonally with respect to the sectors 9, 9′, are provided with highly reflective surfaces. The four sectors 11 lying between the sectors 9, 10, 9′ and 10′ are provided with surfaces which are substantially 100% absorbant to radiation. Typically the surfaces of the sectors 11 are coated with black velvet material.

The shaft 7 is located so that the beam 4 is incident on the outer annular portion of the disc 6 in a locus as shown by the broken circle 112 in Fig. 2, and at an angle of 45° to the plane of the disc. As the disc 6 rotates, the beam 4 will be incident successively on the various sectors. When it is incident upon either of the sectors 9 or 9′, the radiation will pass undeflected along the path 12. When the radiation is incident on either of the sectors 10, 10′, it will be reflected along the path 13, and when incident on the sectors 11 the radiation is absorbed. The chopper thus produces a first train of pulses of radiation along the path 12 and a second train along the path 13, the pulses of the two trains being interlaced, and with dark intervals between successive pulses. The radiation pulse train along the path 12 passes through a reference cell 14 and is deflected by mirrors, 15, 16 to fall on a radiation detector 17, typically a photomultiplier. The radiation pulse train along the path 13 is deflected by a mirror 18 to pass through a sample cell 19 and is then further deflected by mirrors 20, 21 to fall on the radiation detector 17.

It is apparent that the radiation detector 17 will produce an electrical output signal comprising two interlaced trains of pulses, the amplitude $V_R$ of the pulses of the one (reference) train being representative of the intensity $I_R$ of the radiation pulses reaching the detector via the reference cell 14, and the amplitude $V_S$ of the pulses of the other (sample) train being representative of the intensity of the radiation pulses reaching the detector via the sample cell 19. In the intervals between pulses, when no radiation reaches the detector by either route, the dectector output signal has an amplitude $V_D$ (the dark level).

The output from the radiation detector is applied to a clamp circuit 22 which is effective to clamp the signal level during the dark intervals at zero potential i.e. to make $V_D = 0$. The signal appearing at the output terminal 23 of the clamp circuit 22 is therefore a composite signal of the form shown in Fig. 4 at (a).

A gate pulse generator indicated generally by the reference, 24, is associated with the chopper 5, and comprises an encoder disc 25 mounted on the shaft 7 for rotation synchronously with the chopper disc 6. As shown in Fig. 3 the disc 25, which is generally opaque, is notionally divided into sectors corresponding to the sectors of the disc 6.

In the sectors 26, 26′ corresponding respectively to the sectors 9, 9′ of the disc 6, there are provided translucent annular slots 27, 27′, at a radius $r_R$ from the centre of the disc. Similarly, in the sectors 28, 28′ corresponding to sectors 10, 10′ of the disc 6, there are provided translucent annular slots 29, 29′ at a radius $r_S$ from the centre of the disc 25. In each of the sectors 30, corresponding to the sectors 11 of the disc 6, there is provided a translucent annular slot 31 at a radius $r_D$ from the centre of the disc 25.

At one side of the disc 25 there is provided a light source 132, and at the other side a detector array 133 comprising three light detectors, e.g. photodiodes, the arrangement being such that light passing through the slots 27 falls only on a first photodiode, light passing through the slots 29 falls only on a second photodiode and light through the slots 31 falls only on a third photodiode. Consequently, as the disc 25 is rotated in synchronism with the chopper, the first photodiode produces a train of gate pulses $G_R$ in synchronism with the reference radiation pulses, the second photodiode produces a train of

gate pulses $G_S$ in synchronism with the sample radiation pulses, and the third photodiode produces a train of gate pulses $G_D$ in synchronism with the dark pulses. In each case, the angular extent of the slots 27, 29 and 30 is made somewhat less than the angular width of the corresponding sectors of the chopper disc 6 so that the respective gate pulses are narrower than and lie wholly within the corresponding pulses of the composite signal from the clamp circuit 22. Moreover the output signals from the three photodiodes may be amplified and limited in conventional fashion to provide substantially square-edged gate pulses as shown in Fig. 4 at (b) for the reference gate pulses $G_R$, at (c) for the sample gate pulses $G_S$ and at (d) for the dark gate pulses $G_D$.

The foregoing description is merely exemplary. It will be apparent to those skilled in the art that other optical arrangements may be employed in a dual beam spectrophotometer to produce a composite output signal of the type described and of the form shown in Fig. 4 at (a), and also that other gate pulse generating systems may be employed to produce reference, sample and dark gate pulse trains of the type described and of the form shown in Fig. 4 at (b), (c) and (d).

In the embodiment of a signal processing circuit incorporated in the dual beam spectrophotometer according to the invention and shown in Fig. 1, the composite signal appearing at the output terminal 23 of the clamp circuit 22 is applied to an input terminal 32 of a logarithm circuit 33 to be described in more detail hereinafter, which is effective to produce at its output terminal 34 a composite log signal representative of the logarithm, to the base ten, of the amplitude of the composite signal. This signal is applied to an input of an amplifier 35 which produces at its output terminal 36 an amplified composite log signal.

The output terminal 36 is connected to respective input terminals 37 and 38 of sample-and-hold circuits 39 and 40 which will be described in more detail hereinafter. The reference gate pulse train $G_R$ is applied to a gate input terminal 41 of the circuit 39, which therefore samples the amplified log composite signal only during reference gate pulses. The circuit 39 therefore produces at its output terminal 42 a d.c. signal of amplitude proportional to $\log_{10} V_R$, representative of the logarithm of the amplitude of the reference pulses contained in the composite signal. The sample gate pulse train $G_S$ is connected to a gate input terminal 43 of the circuit 40. This circuit therefore samples the amplified log composite signal only during sample gate pulses, and produces at its output terminal 44 a d.c. signal of amplitude proportional to $\log_{10} V_S$, representative of the logarithm of the amplitude of the sample pulses contained in the composite signal.

The terminals 42 and 44 are connected respectively to a positive input terminal 45 and a negative input terminal 46 of a difference amplifier 47, which produces at its output terminal 48 a signal representative of $\log_{10} V_R - \log_{10} V_S = A$, the absorbance of the sample.

In this arrangement, the low-level signals, whether relating to the reference pulses or the sample pulses, follow a common path. It follows that any error components due to low frequency noise and/or drift in the low signal level stages will be common-mode signals and will be rejected by the difference amplifier 47. Any such signals generated in the sample-and-hold circuits 39 and 40 will be negligible in comparison with the relatively high level of the wanted signals in these stages. Consequently, the effect of low-frequency noise and drift on the absorbance signal A is substantially less than in previously known arrangements.

A preferred circuit arrangement for the logarithm circuit 33 is illustrated in Fig. 5 and comprises an operational amplifier 50, typically Type 741. The input terminal 32 of the circuit 33 is connected to an inverting input 51 of the amplifier 50 via an input resistor 52. A feedback path for the amplifier 50 comprises an n-p-n transistor 53 having its emitter connected to an output terminal 54 of the amplifier 50 and its collector and base connected in parallel to the input terminal 51. The transistor 53 therefore functions as a semiconductor diode.

The voltage versus current characteristic of a semi-conductor diode can be shown to have the form:—

$$V = M \log_{10} (I - I_S) + NI + C \qquad \text{(Eq.1)}$$

wherein I is the current which flows when a potential V is applied across the junction, M, N and C are constants and $I_S$ is a saturated current which flows when V is large and negative i.e. $I_S$ is the reverse leakage current of the junction.

For a silicon junction, $I_S$ is typically of the order of 2nA.

In the present embodiment, I may vary over a range of 0.5$\mu$A to 0.5mA (corresponding to a range of 3 decades in the magnitude of the signal applied to the input terminal 32. $I_S$ may therefore be regarded as negligible by comparison with I, and Equation 1 may be simplified to the form;—

$$V = M \log_{10} I + NI + C \qquad \text{(Eq.2)}$$

It may be noted that, if it were required to operate at lower values of I, a current equal in magnitude to $I_S$ but of opposite sense could be injected into the junction, and the simplified Equation 2 would then still be applicable.

The log multiplying factor M has a value of approximately $60 \times 10^{-3}$ at 20°C thus giving a log law of 60mV per decade change of input current.

The constant N has a value equal to the effective series resistance of the semiconductor junction. It is apparent that if the product NI has a value which is a significant proportion of 60mV when I has its maximum operational value (i.e. 0.5mA), the log law characteristic of the circuit 32 will be distorted at its high current end. It is found that most semiconductor diodes exhibit significantly high series resistance. Although diodes specially constructed to exhibit a low series resistance are available, such log diodes are expensive. It is therefore preferred to employ a transistor 53 connectedias shown in Fig. 5 in place of a diode. In this configuration, the transistor 53 functions as a diode in which the effective series resistance is reduced by the action of the transistor.

Instead of connecting both the collector and the base of the transistor 53 to the input terminal 51 of the amplifier 50, the so called "transdiode" configuration may be employed, wherein the collector of transistor 53 is connected to the terminal 51 and the base is connected to ground. Since the terminal 51 is a virtual earth, the base and collector are effectively connected together, and produce an effect similar to the arrangement of Fig. 5.

In either configuration a maximum current of 0.5mA gives a value for the product NI which is negligible compared with 60mV, and hence the distortion of the log law characteristic is also negligible. Equation 2 canibe rewritten in the form:—

$$V = M \log_{10} I + C \qquad \text{(Eq.3)}$$

The fixed voltage component C in Equation 3 represents the base to emitter voltage $V_{BE}$ of the transistor 53 and typically has a value of 0.5V at 20°C. To reduce the resulting offset in the output signal from the circuit 33, a further diode-connected transistor 55 supplied with a constant current is connected so as to produce a similar offset in the opposite sense. The transistor 55 has its emitter connected to the output terminal 54 of the amplifier 50. Resistors 56 and 57 are connected in series between a positive supply line and the collector of transistor 55. A zener diode has its positive pole connected to the junction of resistors 56 and 57 and its negative pole connected to the emitter of transistor 55. The base of transistor 55 is connected to its collector, which is further connected to the output terminal 34 of the circuit 33. The current through the transistor 55 is therefore determined by the potential across the resistor 57 and the value of that resistor i.e. by the zener voltage $V_Z$ minus the base/emitter voltage of transistor 55 divided by the value of the resister 57. Typically $V_Z = 5.6V$, $V_{BE} = 0.5V$ and $R_{57} = 10Kohm$, giving a constant current of 0.51mA, substantially equal to the maximum value of the current I through the transistor 53. The base/emitter voltage of transistor 55 is of opposite polarity to the component C at the output of the amplifier 50.

To ensure that their respective base/emitter voltages shall be closely similar and shall show similar variations with respect to temperature, the transistors 53 and 55 may be of the same type. Preferably the transistors 53 and 55 are respectively halves of a dual transistor, e.g. Type BCY 89.

The logarithm circuit 33 therefore has a characteristic of the form $V = M \log_{10} I$.

If self-calibration means are added to the signal processing circuit of Fig. 1, as will be discussed later with reference to Fig. 8, then the amplifier 35 may be a variable gain amplifier and may preferably be of the form shown in Fig. 6. The signal from the logarithm circuit 33 is applied to a non-inverting input 59 of an operational 60, typically Type 741. A feedback circuit comprises resistors 61 and 62 and a field effect transistor 63 which may be of Type E112 connected in series between an output terminal 64 of the amplifier 60 and ground, with junction of the resistors 61 and 62 being connected to an inverting input of the amplifier 60. The gate of the F.E.T. 63 is connected to a source of gain control voltage, GVC, via resistor 65, and a further resistor 66, equal in value to resistor 65 is connected between the drain and the gate F.E.T. 63. As the gain control voltage is taken more positive the F.E.T. conducts more heavily, thus shunting an increasing proportion of the feedback signal and so increasing the signal gain of the amplifier. The resistor 62 is provided to limit the maximum gain of the circuit when the F.E.T. 63 is turned hard on. The purpose of the resistors 65 and 66 is to superimpose on the gain control signal a voltage equal to half the drain voltage of the F.E.T. 63. This has the effect of reducing the change of resistance of the F.E.T. with change of drain voltage and so making the resistance of the F.E.T. and with it the circuit gain, more nearly independent of the signal level at the input of the amplifier 60.

The sample-and-hold circuits 39 and 41 may each be of the form shown in Fig. 7. The incoming signal from the amplifier 35 is applied to a source electrode of an N-channel field effect transistor 67. The drain electrode of the transistor 67 is connected via a resistor 68 to one terminal of a capacitor 69 whose other terminal is connected to ground.

A diode 70 has its anode connected to the gate electrode of the transistor 67 and its cathode connected to a source of gating pulses. In the case of circuit 39, the reference gate pulses $G_R$ from the gate pulse generator

24 (Fig. 1) are applied to the cathode of the diode 70. In the case of circuit 40 it is the sample gate pulses $G_S$ which are applied to this point.

A high input-impedance buffer circuit 73, which typically comprises a Type 741 operational amplifier arranged as a unity-gain non-inverting amplifier has its input connected to the junction of the resistor 68 and the capacitor 69.

In the absence of a positive-going gate pulse, the gate electrode of the transistor 67 is held negative by the gate pulse generator via the diode 70 and the transistor is cut off, isolating the capacitor 69 from the input signal. During a positive going gate pulse, the diode 70 is cut off, allowing the gate electrode to be pulled by resistor 72 up to the potential of the input signal, turning on the transistor 67. The capacitor 69 therefore charges, via this transistor and the resistor 68, to the signal potential. During the interval between the end of a first gate pulse and the commencement of a second gate pulse, when the transistor 67 is again cut off, the capacitor 69 remains charged to the potential of the signal during the first gate pulse, save for any droop due to leakage current through the transistor 67 and loading by the buffer 73. Because the leakage of an N-channel F.E.T. is small when its gate electrode is biassed beyond cut-off, and the input impedance of the buffer 73 is high, the droop occuring between successive gate pulses is negligible, and the output of the buffer 73 is a substantially constant potential equal to the potential to which the capacitor 69 charges during gate pulses.

In the case of the circuit 39, this potential is representative of $\log_{10} V_R$ and in the case of the circuit 40 is representative of $\log_{10} V_S$. Consequently the output of the difference amplifier 47 is representative of $\log_{10} V_R - \log_{10} V_S = A$, the absorbance of the sample.

In an alternative arrangement, the sample-and-hold circuits 39 and 40 and the difference amplifier 47 may be replaced by a comparator circuit with internal storage capacity for sampled values of the signal appearing at the output of the amplifier 35. In this arrangement, the output of the amplifier 35 is connected via a first electronic switch (e.g. an F.E.T.] responsive to the pulses of the reference gate pulse train $G_R$ to a first input of the comparator circuit and via a second electronic switch responsive to the pulses of the sample gate pulse train $G_S$ to a second input of the comparator circuit, the absorbance signal A appearing at an output of the comparator circuit.

The comparator circuit may include means for converting the analogue signals at its first and second inputs to respective digital signals and means for forming a digital output signal corresponding to the arithmetic difference between the said digital input signals. The digital output signal may be employed to drive a digital display or print-out of the measured value of the absorbance.

The value of the multiplication factor M (see Equation 3 supra) in the characteristic of the logarithm circuit 33 is directly proportional to the absolute temperature of the semiconductor diode junction. Typically, M varies by $0.21 \times 10^{-3}$ per °C from its value of $60 \times 10^{-3}$ at 20°C. Consequently, the gain of the circuit 33 varies in like manner with the temperature of the semiconductor junction, which will itself vary with changes in ambient temperature.

Any residual offset voltages in the circuit 33 will tend to distort the log law characteristic for low levels of input signal.

Self-calibration circuitry which may be added to the circuit of Fig. 1, including means for maintaining the overall gain substantially constant despite changes in the gain of the logarithm circuit with temperature and means for compensating residual offset voltages will now be described in general terms before a detailed description is given with reference to Figs. 8 and 9 of a complete signal processing circuit including such self-calibrating circuitry.

First, second and third calibration signals whose amplitudes correspond respectively to an upper limit, a mean and a lower limit of the range of signal amplitudes (typically three decades) contained in the composite electrical signal are periodically injected at the input of the logarithm circuit 33. The amplified composite log signal at the output of the amplifier 35 is sampled synchronously with the injection of the calibration signals by respective sample and hold circuits to produce first, second and third d.c. log calibration signals.

The first and second d.c. log calibration signals are compared to produce a first difference signal and the second and third d.c. log calibration signals are compared to produce a second difference signal.

The magnitude of the first difference signal is dependent on the gain of the logarithm circuit, i.e. on the actual value of the multiplying factor M, but is largely insensitive to residual offset voltages, since both the first and second calibration signals are relatively large. The first difference signal is compared with a gain reference signal corresponding to the nominal value of the factor M, and the resulting d.c. error signal is employed to control the gain of the amplifier 35 in such a manner as to reduce the magnitude of the resulting signal.

The magnitude of the second difference signal is very sensitive to residual offset voltages in the logarithm circuit 33. The second difference signal is compared with a reference signal corresponding to zero offset, and any resulting d.c. error signal is fed back to the input of the logarithm circuit 33 to produce a

compensating offset of the opposite sense.

The calibration signals are injected into the logarithm circuit 33 during the dark periods when the value of the composite electrical signal fed to the circuit 33 from the spectrophotometer is clamped at zero. Consequently, calibration components of the amplified composite log signal are not sampled by the circuits 39 and 40 which are gated off during dark periods.

A complete signal processing circuit including self-calibration circuitry as described above will now be described in greater detail with reference to Figs. 8 and 9, wherein integers described hereinbefore are accorded the same reference numerals as in Figs. 1–7.

Referring first to Fig. 8, the logarithm circuit 33, amplifier 35, sample-and-hold circuits 39 and 40 and difference amplifier 47 are as described hereinbefore.

A three-stage ring counter 74 has applied at its input the dark gate pulse train $G_D$ (d, Fig. 4) and produces at a first output a pulse train $G_{D1}$ (e, Fig. 4) corresponding to the 1st, 4th, 7th etc pulses of the train $G_D$. At a second output the counter 74 produces a pulse train $G_{D2}$ (f, Fig. 4) corresponding to the 2nd, 5th, 8th etc pulses of the train $G_D$. At a third output the counter 74 produces a pulse train $G_{D3}$ (g, Fig. 4), corresponding to the 3rd, 6th, 9th etc pulses of the train $G_D$. An invertor 104 also has the dark gate pulse train $G_D$ applied to its inputs and produces at its output the inverse waveform $\bar{G}_D$.

A calibration signal generator, to be described in more detail hereinafter, is represented by the broken rectangle 75 and comprises a signal source 76 producing a first calibration signal C1 corresponding to the high end of the decade range of signals which the apparatus is required to handle, a signal 77 producing a second calibration signal C2 corresponding to the centre of the range, and a signal source 78 producing a third calibration signal C3 corresponding to the low end of the range. For a spectrophotometer having a measurement range of three absorbance units, i.e. from 0A to 3A, the signal range before logging is three decades, and the relative magnitude of C1, C2 and C3 is 1000/31.6/1.

The output signal C1 from the source 76 is connected to the input 51 of the logarithm circuit 33 via a switch 79 arranged to be closed only during pulses of the pulse train $G_{D1}$. Similarly, the signal C2 from the source 77 is connected to the input 51 of the circuit 33 via a switch 80, closed only during pulses of the pulse train $G_{D2}$, and the output C3 from the source 78 is connected to the said input 51 via a switch 81 closed only during pulses of the pulse train $G_{D3}$. The individual calibration signals reaching the said input are shown in Fig. 4 at h, j and k respectively, and the resulting composite signal applied to the logarithm circuit 33 is as shown in Fig. 4 at 1.

A more detailed schematic diagram of a calibration signal generator unit 75 is shown in Fig. 9 which it is seen than an N channel F.E.T. is used for each of the switches 79, 80, 81 each transistor being arranged to conduct when its gate electrode is taken positive by the respective gate pulses $G_{D1}$, $G_{D2}$ or $G_{D3}$.

The signal source 76 is a stabilised reference voltage supply. When switched on, the F.E.T. 79 connects the reference voltage to the virtual earth input of the amplifier 50 in the logarithm circuit 33 via a resistor 82, equal in value to the input resistor 52 of the logarithm circuit. The reference voltage, i.e. C1 represents absorbance 0A.

The signal source 77 comprises resistors 83 and 84 connected in series between the reference supply and ground, so as to divide down the reference voltage by a factor of 31.6 to provide the second calibration signal C2 representing absorbance 1.5A. The F.E.T. 80, when switched on, connects the second calibration signal C2 to the input amplifier 50 via a resistor 85.

Similarly the signal source 78 comprises resistors 86 and 87 which divide down the reference voltage by a factor of 1000 to provide a third calibration signal C3 representing absorbance 3.0A. The F.E.T. 81, when switched on, connects the third calibration signal C3 to the input of amplifier 50 via the resistor 85.

The value of the resistor 85 is chosen so that it, with the potential divider chain 83 and 84, or 86 and 87 as the case may be presents the same impedance at the input of the amplifier 50 as does the resistor 82. In order that the same impedance shall be presented to the input of the amplifier 50 whether calibration signals are present or not, a further F.E.T. 88 is provided and is fed with the switching waveform $\bar{G}_D$ which is the inverse of the dark gate pulse train $G_D$. The F.E.T. 88 is therefore cut off during all dark pulses, but is conductive during reference and sample pulses. When conductive the F.E.T. 88 connects the resistor 82 between the input of the amplifier 50 and ground.

Reverting now to Fig. 8, calibration signal decoding and processing circuits are shown within the broken rectangle 89. Three sample-and-hold circuits, 90, 91 and 92 are provided, each of the type described hereinbefore with reference to Fig. 7. Each of the circuits 90, 91 and 92 has its signal input connected to the output of the amplifier 35.

The gate pulse train $G_{D1}$ is applied to the gate input of the circuit 90, which therefore produces at its output a first d.c. log calibration signal proportional to $\log_{10}$ C1, representative of an absorbance 0.A. Similarly, the circuit 91 is gated by the pulse train $G_{D2}$ and produces at its output a second d.c. log

calibration signal proportional to signal $\log_{10}$ C2, representative of an absorbance 1.5A. The circuit 92 is gated by the pulse train $G_{D3}$ and produces at its output a third d.c. log calibration signal proportional to $\log_{10}$ C3, representative of an absorbance 3.0A.

The signal from the circuit 90 is applied to a non-inverting input of a difference amplifier 93, and the signal from the circuit 91 is applied to an inverting input of the amplifier 93, which therefore produces a first difference signal. The output of the amplifier 93 is connected to an input of an integrator circuit 94 via a resistor 95. A further resistor 96 is connected between a stabilised reference potential source 97 and the input of the integrator 94, it being arranged that the reference current flowing to the integrator input via the resistor 96 is of magnitude corresponding to a change of absorbance from A = 0 to A = 1.5 and is of opposite sense to the first difference current flowing to the input via the resistor 95.

The output of the integrator 94 is connected to the gain control voltage input of the amplifier 35 (see Fig. 6).

If the first difference current is less than the reference current, the integrator 94 produces an output potential effective to increase the gain of the amplifier 35, which in turn causes the first difference current to increase until it equals the reference current, and the nett input current to the integrator 94 becomes zero. The integrator output then becomes constant and holds the gain of the amplifier 35 constant. Similarly, if the output difference current exceeds the reference current, the integrator 94 produces an output potential of the opposite polarity which is effective to reduce the gain of the amplifier 35 until the nett input to the integrator 94 is again reduced to zero, whereafter the gain is held constant, In this manner, any change in gain of the logarithm circuit 33 is balanced by a corresponding change, in the opposite sense, of the gain of the amplifier 35, and the overall gain is constant.

Compensation for residual offset voltages in the logarithm circuit 33 is provided in a somewhat similar manner. The second d.c. log calibration signal from the circuit 91 is applied to a non-inverting input of a further difference amplifier 98 and the third d.c. log calibration signal from the circuit 92 is applied to an inverting input of the amplifier 98. The latter therefore produces a second difference signal which is applied to an input of an integrator 99 via a resistor 100. The second difference current flowing into the integrator 99 via the resistor 100 is opposed by a reference current flowing through a resistor 101 connected between the input of the integrator and the stabilised reference source 97, the magnitude of the reference current corresponding to a change in absorbance from A = 1.5 to A = 3.0.

The output of the integrator 99 is connected, via a unity gain invertor 102 and a resistor 103 to the input of the logarithm circuit 33.

If, due to internal offset voltages in the logarithm circuit 33, the second difference current does not equal the reference current at the input to the integrator 99, the latter produces an output signal which drives a current through the resistor 103 and into the input of logarithm circuit 33 which is effective to produce therein an offset voltage of the opposite sense. This process continues until the nett input to the integrator 99 becomes zero, when the output of the integrator becomes constant and the current fed to the logarithm circuit via the resistor 103 stabilises at a value such as to compensate the internal offset voltages, and so correct any distortion of the log law at low signal inputs.

In the specific embodiments of a dual beam spectrophotometer described hereinbefore, the composite output signal of the detector to be processed contains redundant intervals (the dark periods) between successive pulses of the two interlaced pulse trains. It is therefore possible to utilise these redundant periods for the self-calibration of the apparatus and so avoid any loss of the information carried in the composite signal during self-calibration.

A similar method of self-calibration may be employed when there are no redundant intervals in the composite signal.

It can be assumed that the rate of variation of gain and/or offset of the logarithm circuit 33 will be small, and hence the gain control signal from the integator 94 and the offset compensation signal from the integrator 99 need be updated only occasionally. Hence the repetition rate of the calibration gate pulse trains $G_{D1}$, $G_{D2}$ and $G_{D3}$ may be very much smaller than that of either of the pulse trains comprising the composite signal.

Instead of the counter 74 being driven by the dark gate pulse train $G_D$, it may be driven by the output of a further counter, itself driven by the reference gate pulse $G_R$ or the sample gate pulse train $G_S$, and arranged to produce an output pulse for every *n*th pulse applied to its input.

In this way, only 1/n of the information in the composite signal will be lost during calibration, and *n* may be made sufficiently large that this loss is negligible.

CLAIMS

1. A dual beam spectrophotometer comprising a detector for radiation received from a radiation source via a first path including a reference cell and via a second path including a sample cell, the radiation received via the first and second paths being in the form of interlaced pulses separated by periods in which no radiation reaches the detector via

either path, the detector producing a first signal comprising a first train of pulses of amplitude corresponding to the intensity of radiation received via the first path and a second train of pulses of amplitude corresponding to the intensity of radiation received via the second path, the pulses of the first and second trains being interlaced and being separated by the said periods, means for clamping the first signal at a reference level during the said periods to produce a second signal, and a processing circuit for processing the second signal to obtain a further signal representative of the absorbance of a substance contained in the sample cell, characterised in that the processing circuit includes means for producing a third signal representative of the logarithm of the amplitude of the second signal, means for amplifying the third signal to produce a fourth signal, means for sampling the fourth signal to produce a fifth signal representative of the logarithm of the amplitude of the pulses of the first train, and a sixth signal representative of the logarithm of the amplitude of the pulses of the second train, and means for producing said further signal as a seventh signal representative of a difference between the fifth and sixth signals.

2. A spectrophotometer according to Claim 1, in which the means for producing the third signal is a logarithm circuit comprising an operational amplifier, an input resistor connected between an inverting input of the operational amplifier and an input terminal for receiving the second signal, a first transistor connected as a diode between an output of the operation amplifier and the said inverting input, a second transistor connected as a diode between the output of the operational amplifier and an output terminal for the third signal so that the base-emitter potential of the second transistor is of opposite polarity to the potential appearing at the output of the operational amplifier due to the base-emitter potential of the first transistor and means for supplying to the second transistor a constant current substantially equal to the current flowing in the first transistor when the amplitude of the second signal is at its maximum value.

3. A spectrophotometer according to Claim 2, in which the first transistor and the second transistor are respective halves of a dual transistor.

4. A spectrophotometer according to Claim 1, in which the means for amplifying the third signal is a feedback-stabilised variable gain amplifier comprising an operational amplifier having the third signal applied to a non-inverting input thereof, with feedback means connected between an inverting input of the amplifier and a tapping point on a potentiometer chain connected between an output of the amplifier and ground, the potentiometer chain including a field effect transistor with its source to drain path connected in the section of the potentiometer chain between the tapping point and ground, and means for varying the potential of a gate electrode of the field effect transistor to adjust the feedback so as to stabilise the gain of the amplifier at a desired value.

5. A spectrophotometer according to Claim 1, in which the means for sampling the fourth signal comprises two sample-and-hold circuits for respectively sampling the fourth signal at times corresponding to the pulses of the first and second trains and respectively producing the fifth and sixth signals.

6. A spectrophotometer according to Claim 1, in which the means for producing the seventh signal comprises a differential amplifier having the fifth signal applied to a non-inverting input thereof, having the sixth signal applied to an inverting input thereof, and producing the seventh signal at an output thereof.

7. A spectrophotometer according to Claim 1, further comprising means for generating upper and mean calibration signals having respective amplitudes corresponding to an upper limit and a mean limit of a range of pulse amplitudes of the second signal, means for applying the calibration signals to an input terminal of the means for generating the third signal, further means for sampling the fourth signal to produce an eighth signal representative of the logarithm of the amplitude of the upper calibration signal and a ninth signal representative of the logarithm of the amplitude of the mean calibration signal, means for producing a tenth signal representative of a difference between the respective magnitudes of the eighth and ninth signals and means responsive to the tenth signal for controlling the gain of the means for amplifying the third signal so as to maintain the magnitude of the tenth signal substantially constant.

8. A spectrophotometer according to Claim 1, further comprising means for generating mean and lower calibration signals having respective amplitudes corresponding to a mean limit and a lower limit of a range of pulse amplitudes of the second signal, means for applying the calibration signals to an input terminal of the means for generating the third signal, further means for sampling the fourth signal to produce an eighth signal representative of the logarithm of the amplitude of the mean calibration signal and a ninth signal representative of the logarithm of the amplitude of the lower calibration signal, means for producing a tenth signal representative of a difference between the respective magnitudes of the tenth signal for generating an eleventh signal effective when applied to the input of the means for generating the third signal to maintain the magnitude of the tenth signal substantially equal to a predetermined value.

9. A spectrophotometer according to Claim 1 further characterised by means for

generating first, second and third calibration signals having respective amplitudes corresponding to an upper limit, a mean and a lower limit of a range of pulse amplitudes of the second signal, means for applying the calibration signals to an input terminal of the means for generating the third signal, further means for sampling the fourth signal to produce an eighth signal representative of the logarithm of the amplitude of the first calibration signal, a ninth signal representative of the logarithm of the amplitude of the second calibration signal and a tenth signal representative of the logarithm of the amplitude of the third calibration signal, means for producing an eleventh signal representative of a difference between the respective magnitudes of the eighth and ninth signals, means responsive to the eleventh signal for controlling the gain of the means for amplifying the third signal so as to maintain the magnitude of the eleventh signal substantially constant, means for producing a twelfth signal representative of a difference between the respective magnitudes of the ninth and tenth signals and means responsive to the twelfth signal for generating a thirteenth signal effective when applied to the input of the means for generating the third signal to maintain the magnitude of the twelfth signal substantially equal to a predetermined value.

10. A spectrophotometer according to Claim 9, in which the respective amplitudes of the first, second and third calibration signals are in the ratio 1000:31.6:1.

11. A spectrophotometer according to Claim 9, in which the means for applying the calibration signals to the input terminal of the means for generating the third signal comprises first switch means for applying the first calibration signal during a first one of the periods in which no radiation reaches the detector by either the first or the second path, second switch means for applying the second calibration signal during a second one of the said periods, third switch means for applying the third calibration signal during a third one of the said periods and fourth switch means for connecting a load equal to an output impedance of the means for generating the calibration signals to the said input terminal when no calibration signal is applied thereto.

12. A spectrophotometer according to Claim 11, in which the first, second, third and fourth switch means comprise respective field effect transistors which are normally biassed to a non-conducting state and are driven into conduction by respective trains of pulses applied to gate electrodes of the said transistors, said respective trains of pulses being generated from a further train of pulses corresponding to the said periods.

13. A spectrophotometer according to Claim 9, in which the further means for sampling the fourth signal comprises three sample-and-hold circuits for respectively producing the eighth, ninth and tenth signals.

14. A spectrophotometer as claimed in Claim 7, in which the means responsive to the tenth signal is an integrator circuit receiving at an input thereof the tenth signal and a constant reference signal and effective to integrate any difference between the said signals to produce an output signal for use in controlling the gain of the means for amplifying the third signal, the magnitude and polarity of the output signal being such as to control the gain in a sense to minimise the said difference.

15. A spectrophotometer as claimed in Claim 8 in which the means responsive to the tenth signal is an integrator circuit receiving at an input thereof the tenth signal and a constant reference signal and effective to integrate any difference between the said signals to produce the eleventh signal and means for applying the eleventh signal to the input terminal of the means for generating the third signal in such sense as o reduce the difference between the tenth signal and the second reference signal.

16. A spectrophotometer substantially as described herein with reference to Figs. 1 to 7 of the accompanying drawings.

17. A spectrophotometer substantially as described herein with reference to Figs. 1 to 7 together with Figs. 8 and 9 of the accompanying drawings.

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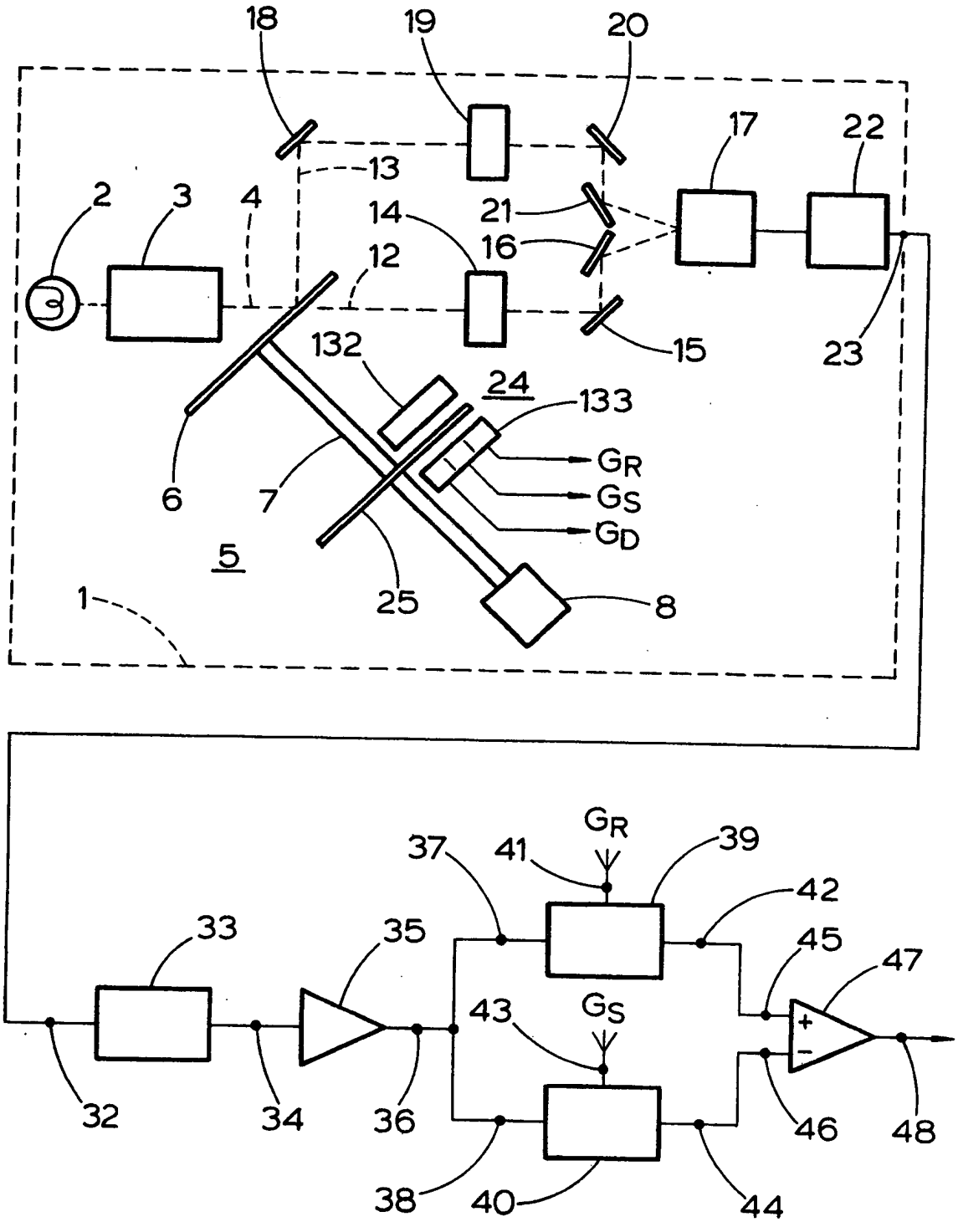
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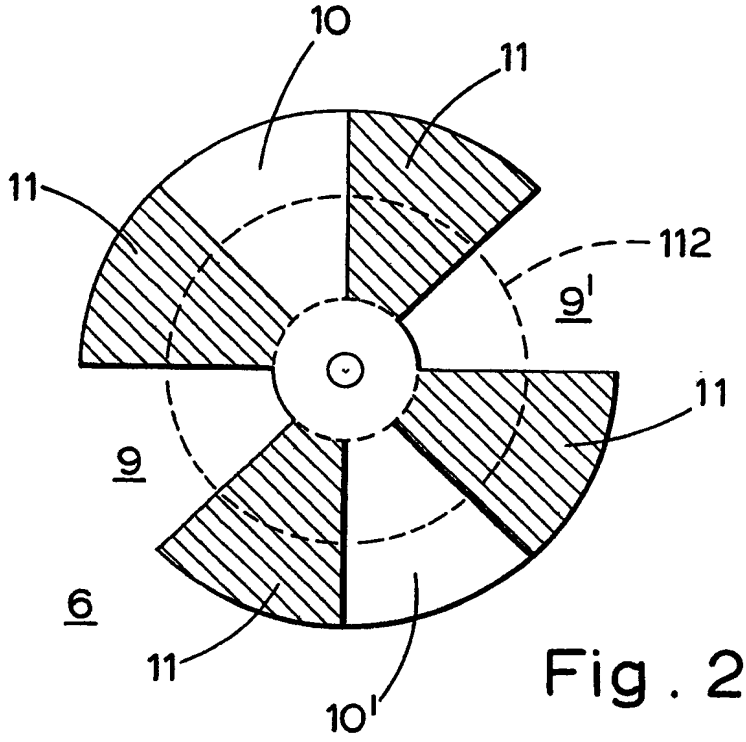
Fig . 1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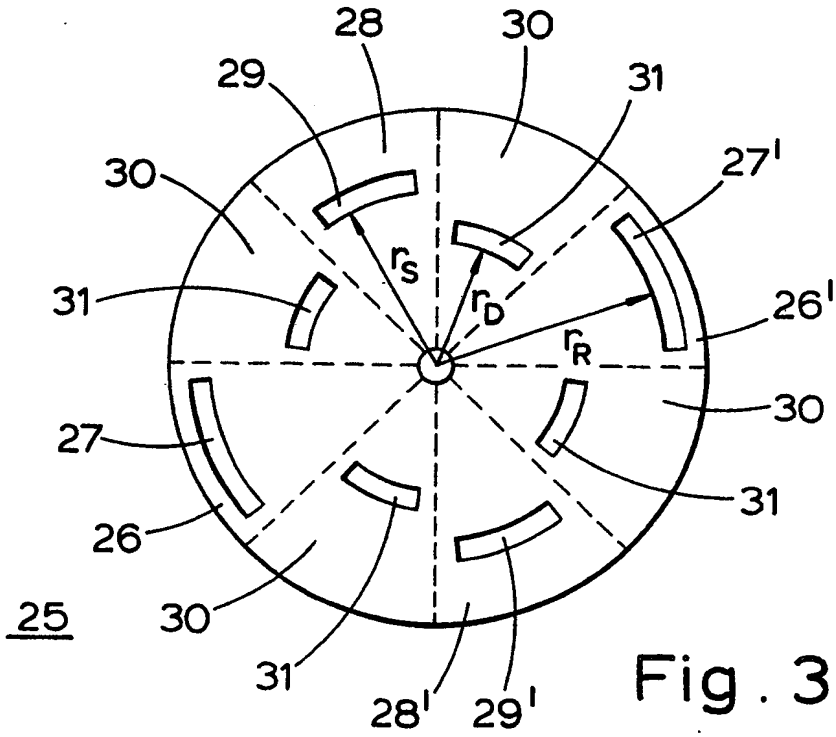
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Fig. 3

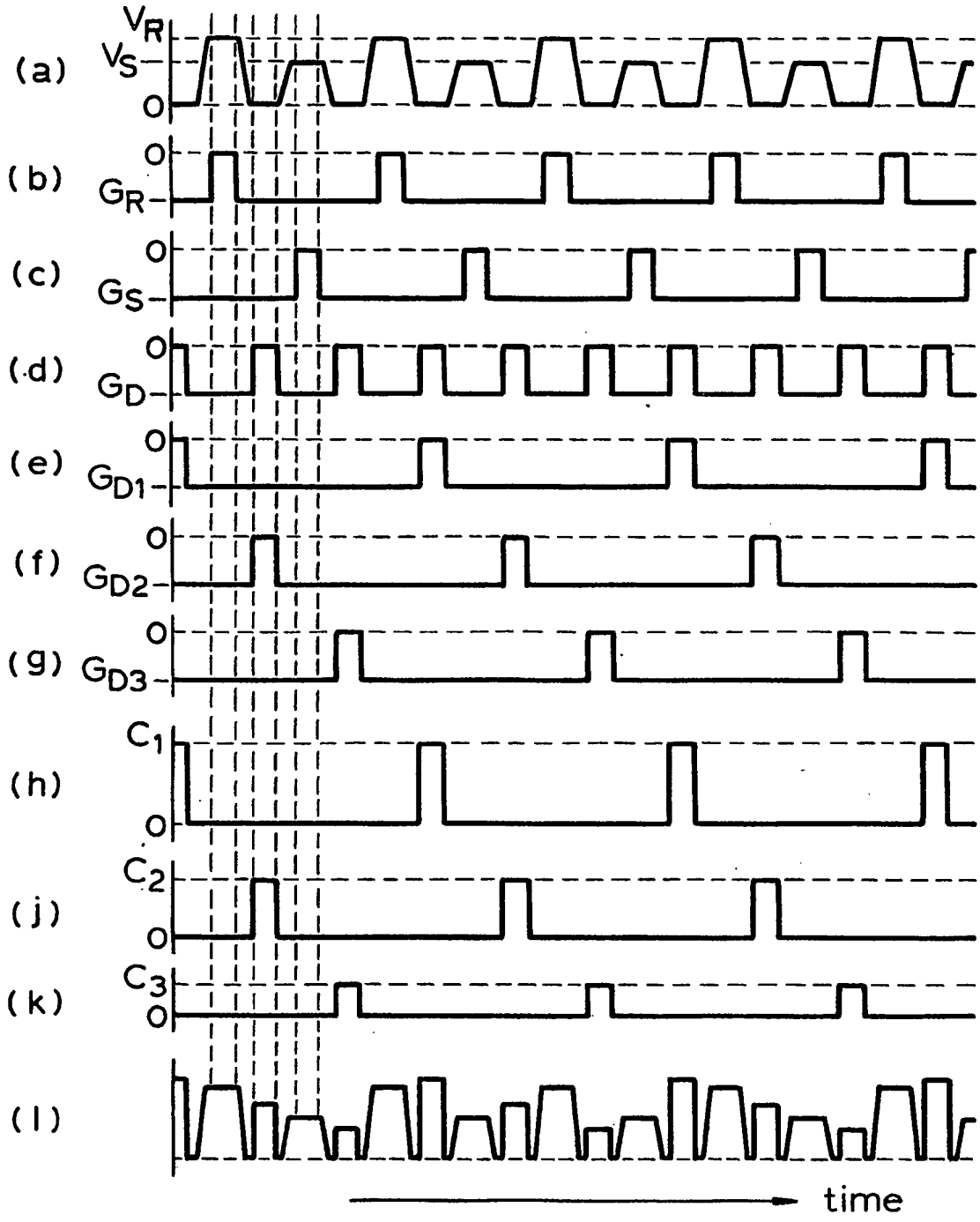


Fig. 4

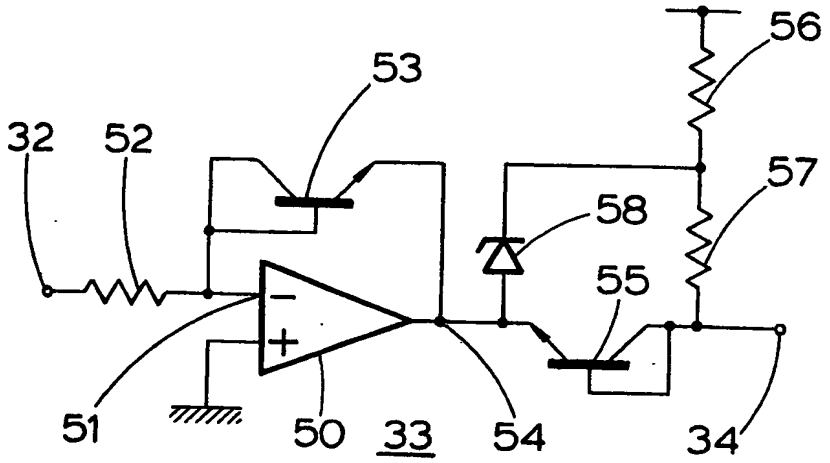


Fig. 5

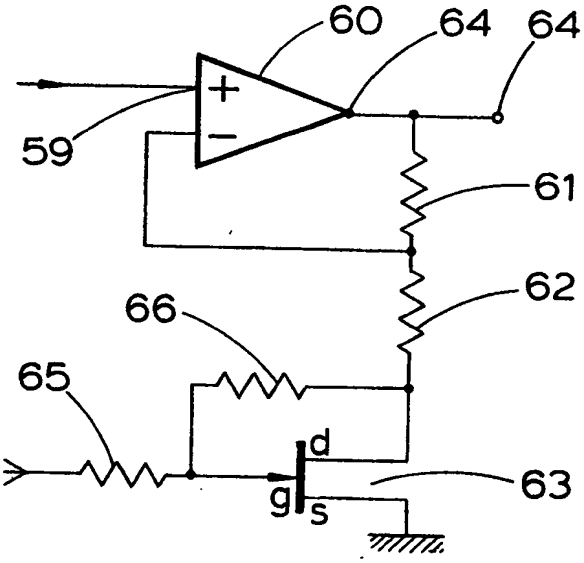


Fig. 6

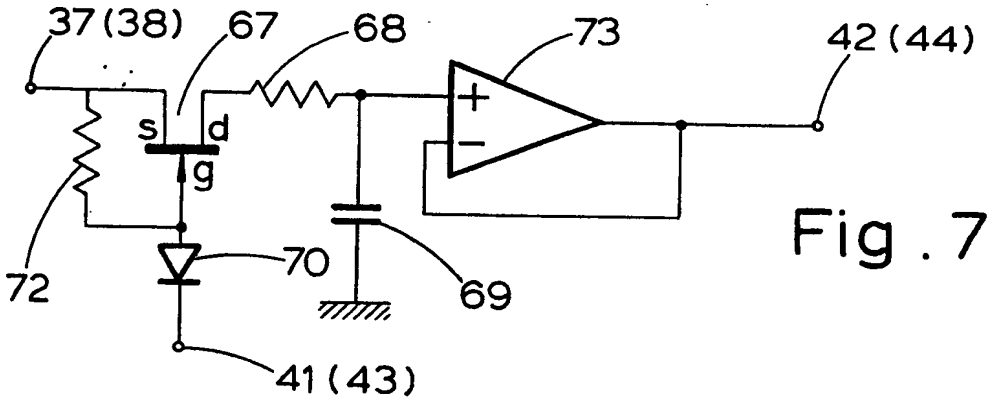


Fig. 7

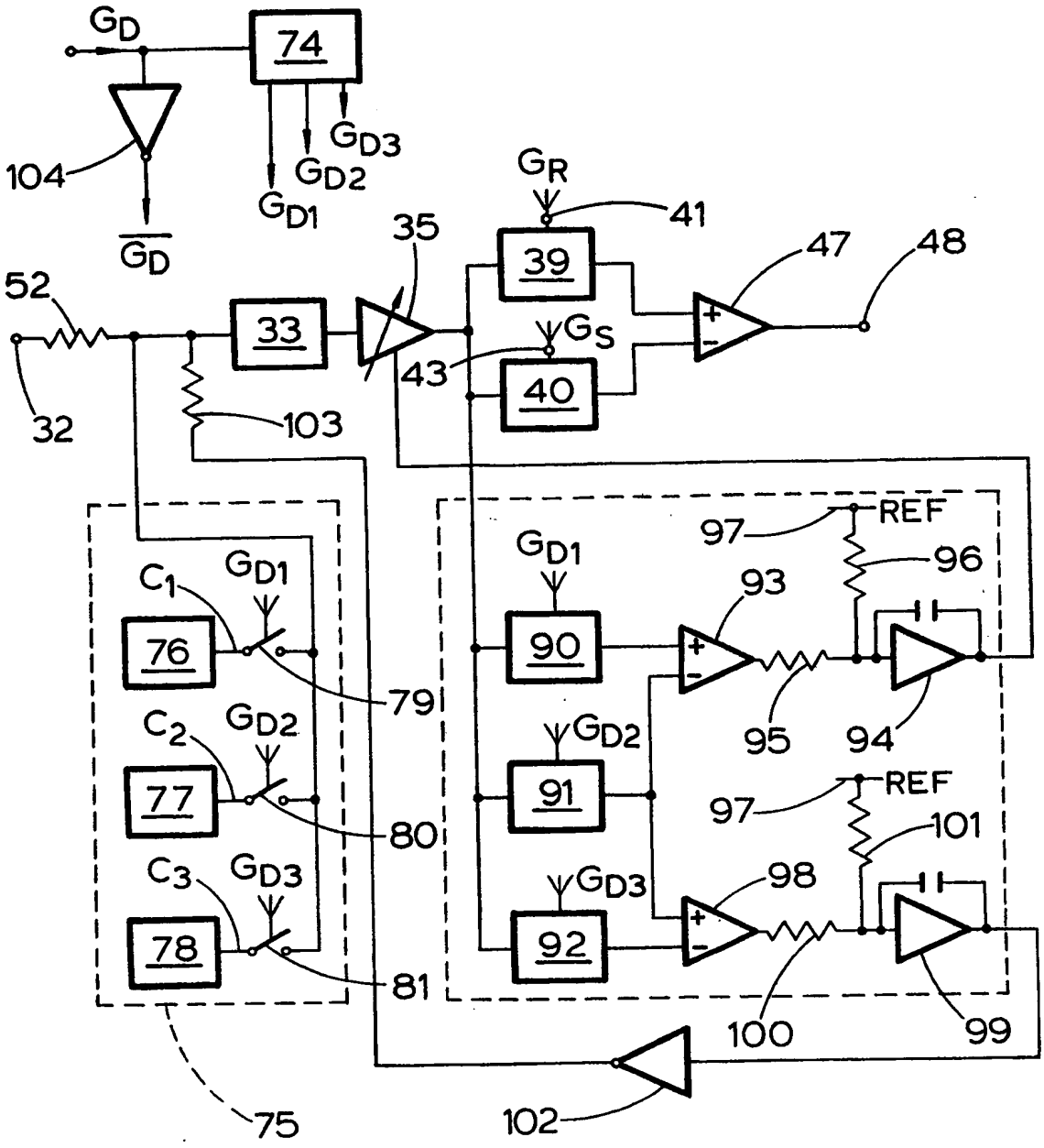
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Fig . 8

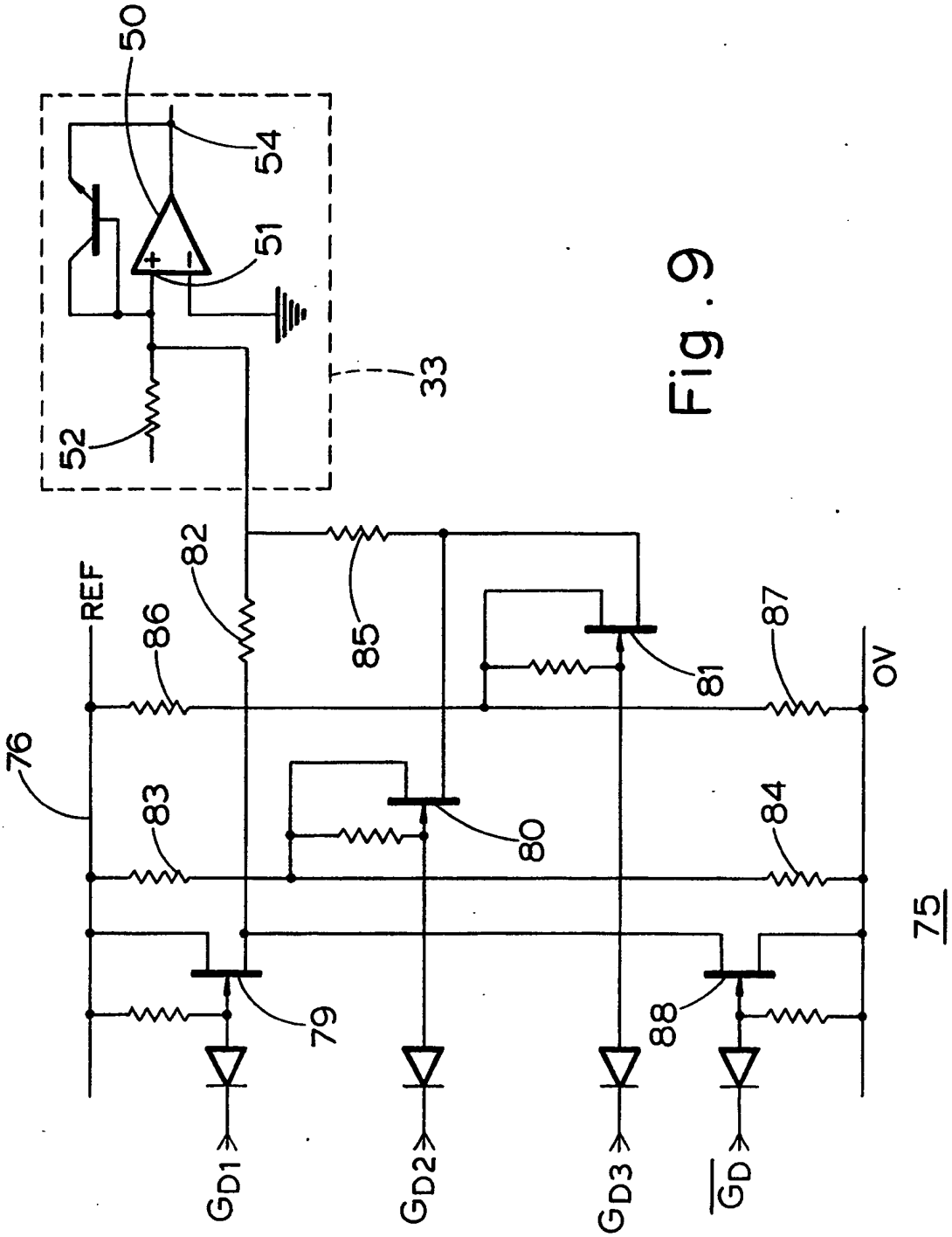
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Fig. 9